ADQ3-FWPD Datasheet

The ADQ3-FWPD is a real-time pulse detection and pulse analysis FPGA firmware for the high-end ADQ3-series digitizers. ADQ3-FWPD adds pulse attribute calculations to the standard firmware FWDAQ.

Ordering information

- Firmware option FWPD for ADQ3-series of digitizer, order code **ADQ3-FWPD**.
- FWPD combined with firmware development kit, **ADQ3-DEVPD** (available 2024)

Compatible hardware models

- ADQ30 single-channel mode
- ADQ32 single- and dual-channel modes
- ADQ32-PDRX combined channels and dual-channel mode (not combined)
- ADQ33 dual-channel mode
- ADQ33-PDRX combined channels and dual-channel mode (not combined)
- ADQ35 single- and dual-channel mode
- ADQ36 in dual- and quad-channels modes

1 ADQ3-FWPD INTRODUCTION

1.1 Features

- Compliant with features of FWDAQ
  - Frame pulses using trigger blocking
  - Detect pulses using level trigger
  - Correct baseline using Digital baseline Stabilizer (DBS)
  - Timestamp for pulse time determination
  - Daisy-chain trigger distribution concept for large arrays of detectors
- Data rate reduction in the FPGA of the digitizer by computing attributes of pulses
- Data and attributes transferred as separate channels for flexible selection of operating mode
- Pulse attribute calculations:
  - Area (sum)
  - Full width half max (FWHM)
  - Time of pulse peak
  - Maximum pulse amplitude
  - Open FPGA allows for customization of attributes

1.2 Applications

- Time-of-flight mass spectrometry
- LiDAR
- Neutron time-of-flight
- High energy physics
- Other types of pulse detection

1.3 Advantages

- Efficient implementation of pulse detection and analysis in the FPGA off-loading the PC
- Optimized for real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2 BLOCK DIAGRAM

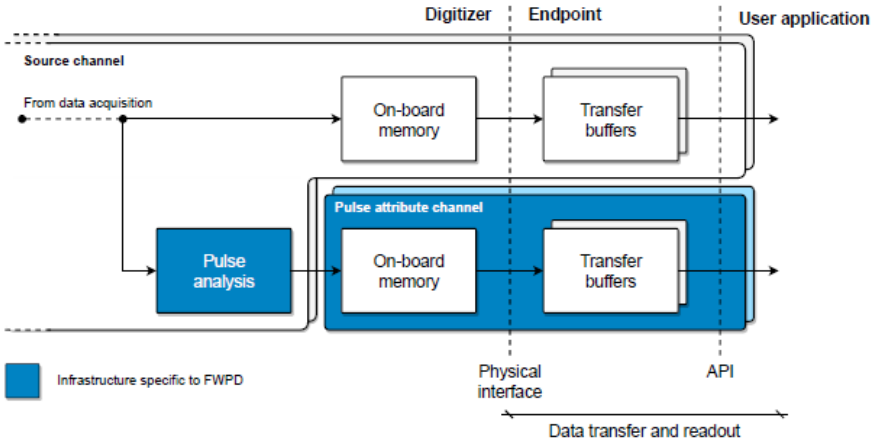

Figure 1 Block diagram of FWPD. FWPD adds attributes computations and attributes channels to the functions in standard firmware FWDAQ.

3 PULSE DETECTION AND ANALYSIS – PRINCIPLE OF OPERATION[1]

3.1 DBS – Digital Baseline Stabilizer

The DBS analyses the signal and subtracts the DC-offset. This creates a stable reference point for computing pulse-related parameters. The DBS actively compensates for slow baseline shifts such as temperature variations, supply voltage drift and aging, and stabilizes the baseline to a level corresponding to 22-bit precision. The DBS also compensates for pattern noise in interleaved ADCs.

3.2 General-purpose FIR filter

The general-purpose FIR filter enables the suppression of noise in a certain frequency band. The FIR filter is user-controlled so that it can be optimized for the specific application/system.

3.3 Detection window

The detection window defines where to search for pulses. It is controlled by an event (trigger) and a length parameter. The detection window is comparable to the term “record” in the standard acquisition mode.

3.4 Pulse detection

Pulse detection is handled by level triggering. The start of a pulse occurs when the signal level is passing a level and end of a pulse occurs when the signal is passing the same level from the opposite direction. The direction is depending on the polarity of the pulse.[2] A leading-edge window and a trailing-edge window define additional samples that belong to the pulse.

3.5 Pulse attributes analysis

A set of standard attributes is calculated for each pulse in FWPD. The attributes can be replaced by custom attributes using the open FPGA.[3]

The 21-2539 user guide of ADQ3 digitizers contains a detailed definition of how the attributes are computed.

- Time of pulse peak
- Area (sum) of pulse
- Full width at half maximum (FWHM)
- Peak amplitude

The attributes are sent to the host PC on a separate attributes channel. The digital output of the board has twice as many channels as analog inputs, data, and attributes per channel.

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[1] All features in this section except for the computation of attributes and the attributes data channel are available in standard firmware FWDAQ.
[2] The polarity of the pulses is set by the user. The FWPD can only handle one polarity per channel.
[3] Open FPGA is accessed through the development kit with order code DEVPD. The DEVPD is available in 2024. Please contact Teledyne SP Devices for more information.

4 SYSTEM DESIGN USING FWPD

4.1 Fundamental observations

FWPD is used in measurement systems where detectors and the digitizer operate in a real-time. The data, on the other hand, is analyzed on a PC, which is not real-time controlled. FWPD is designed to handle the transition between the real-time domain into the PC in a safe way.

4.2 System design optimization - open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high-speed real-time analysis. The ADQ3-series offers a variety of options for efficient system design:

The FWPD firmware implements the most demanding core processing inside the FPGA. Data from the processing is streamed to a PC using the high-speed streaming interface.

The streaming is done in parallel with the recording without introducing any dead-time.

See the ADQ3-series user guide for instructions on how to tune parameters for optimal performance.[4]

4.3 Large arrays of detectors

Use the Daisy-chain trigger distribution for synchronization of large arrays.

4.4 Scheduling for high performance and data safety

FWPD is designed for systems with data-driven operation. The dataflow is driven by pulse activity. The ADQ3-series digitizer contains a large FIFO to smoothen the data flow. The user must ensure that all data transfer and processing is fast enough to handle the average data rate.

FWPD is designed to operate constantly over a long time in order to maximize performance. It contains multiple features to support the necessary data transfer and processing:

1. There is an onboard FIFO to manage unexpected interrupts in the PCIe data transport.
2. There is a controlled data discard in case of an overflow due to interrupts anywhere in the processing chain.
3. There is an auto-recover and resynchronization feature in case of lost data. This is useful for very long measurement operations. In case of an unexpected interrupt in the data transport which cannot be handled by the FIFO, the FWPD firmware maintains the grid established by the trigger source. It is not necessary to restart the system to continue the measurement.
4. The data readout is thread-safe and multiple threads can operate on the data. This increases the processing capacity of the system.

[4] ADQ3-series user guide with document number 21-2539 can be downloaded from www.spdevices.com

5 TECHNICAL DATA

Table 1 Pulse detection

Parameter	Description	Limitation
Pulse spacing	Distance between two consecutive pulse peaks	Min 2 samples
Pulse rate	Maximum sustained rate for ADQ32, ADQ35, ADQ36	Max 312.5 Mpulses per second[5]
Pulse rate	Maximum sustained rate for ADQ30, ADQ33	Max 125 Mpulses per second[5]
Burst length	Burst of pulses exceeding average long-term pulse rate	Max 256 pulses
Burst length for ADQ35 in 1-channel mode	Additional burst length requirement for ADQ35 in 1 channel mode	Max 8 pulses per set of 32 samples

Table 2 Attributes

Attribute	Description	Size [bytes]
Time	Time of peak value	4
Area	Area (sum) of pulse	4
FWHM	Full width half max	2
Peak value	Value of largest sample	2
Reserved	Reserved	4

[5] This is the capacity of the analysis firmware. Note that there is also a data transfer limit over PCIe of the hardware.

Table 3 Limitations on computations of attributes

Model	Channels	Sampling rate [GHz]	FWHM max		Area computation	
			Time [us]	Length [samples]	Max LEW [6] [Samples]	Max TEW [7] [Samples]
ADQ30	1	1	4.1	4096	64	64
ADQ32	2	2.5	3. 3	8192	64	64
ADQ32	1	5	3.3	16384	64	64
ADQ32-PDRX	1	2.5	3.3	8192	64	64
ADQ33	2	2.5	4.1	4096	64	64
ADQ35	2	5	3.3	16384	64	64
ADQ35	1	10	3.3	32768	64	64
ADQ35-PDRX	1	5	3.3	16384	64	64
ADQ36	4	2.5	3.3	8192	64	64
ADQ36	2	5	3.3	16384	64	64

Table 4 Software support

Parameter	Value
Operating system[8]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[6] LEW is leading edge window, that is, the number of samples before passing the threshold at the start of the pulse.

[7] TEW is trailing edge window, that is the number of samples after passing the threshold at the end of the pulse.

[8] See 15-1494 Operating system support for a detailed listing of supported distributions.

Table 5 Data transfer rate

Mode	Description	Data set per trigger[9]
Continuous recording[10] of original signal	Continuous recording of raw data from original signal	PCIe transfer rate limits the recording
Detection window /record[10]	All data within a detection window is recorded as one record	Record length + header[11]
Pulse detection / zero suppression[10]	Samples which belong to pulses are recorded	Average number of pulses * (header[11] + average pulse length)
Pulse attributes[12]	Computed attributes of pulses	Header[11] + 16 bytes * average number of pulses[13]

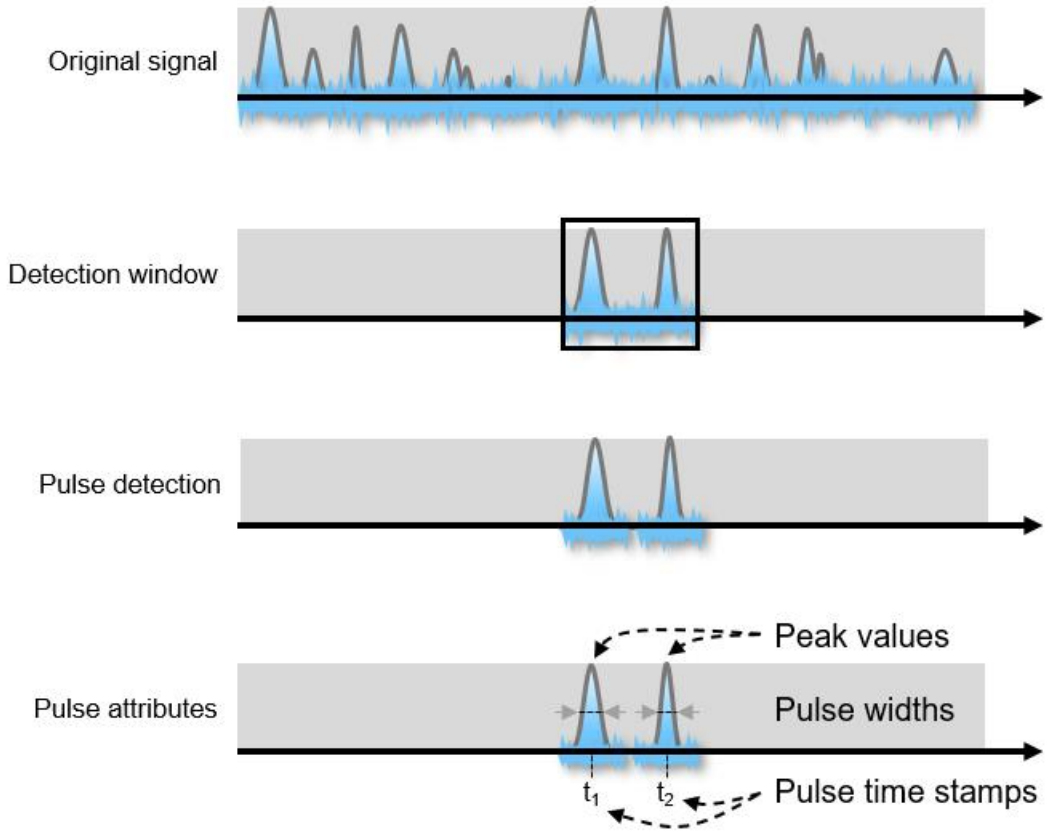

Figure 2 Pulse detection and analysis

[9] Average data rate is trigger rate multiplied with size of data set.
[10] Available in FWDAQ and FWPD.
[11] The header is 72 bytes.
[12] Requires FWPD. Not available in FWDAQ.
[13] Each pulse result in 16 bytes of attribute data

6 CHANGING NUMBER OF CHANNELS

Some hardware models support both one and two channels operation. Changing from two channels to one channel is done by changing firmware image in the FPGA. Both firmware images are stored in the non-volatile memory of the digitizer. Use the software tool ADQAssist to change boot image. Changing firmware requires power cycling of the PC for the PCIe bus to enumerate.

7 BLOCK DIAGRAM

Below are block diagrams for FWPD installed in various hardware configurations.

The User Logic 1 and User Logic 2 blocks are available for the user through the Firmware Development Kit, DEVPD, which is ordered separately and available in 2024.

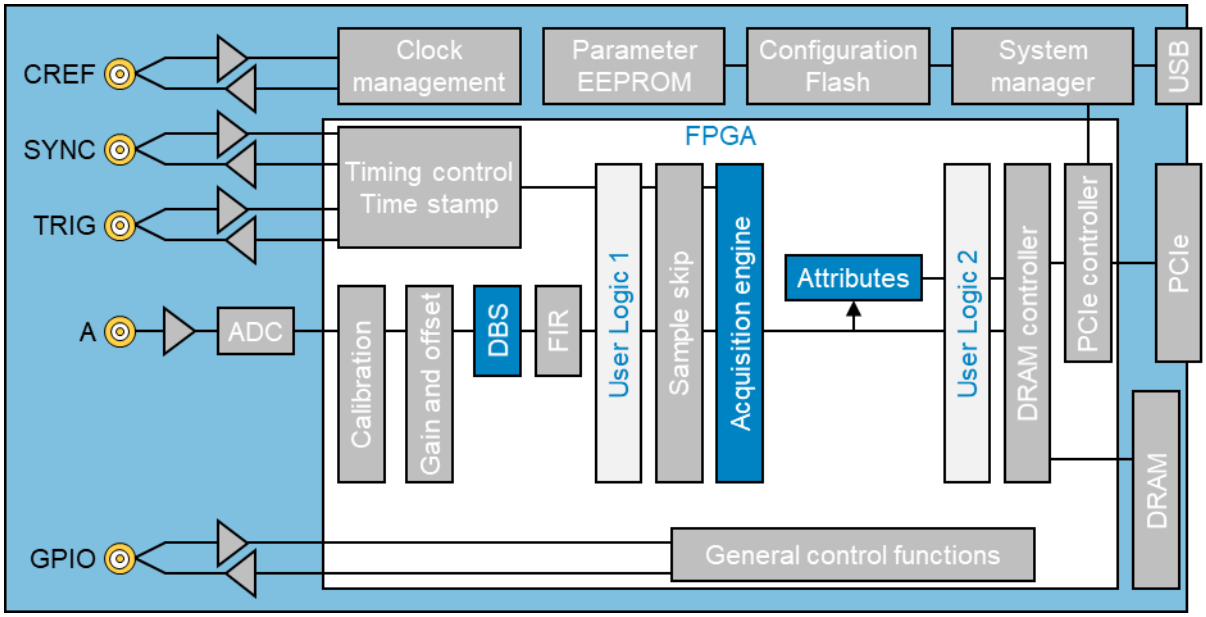

Figure 3 Block diagram for FWPD installed on a single-channel digitizer.

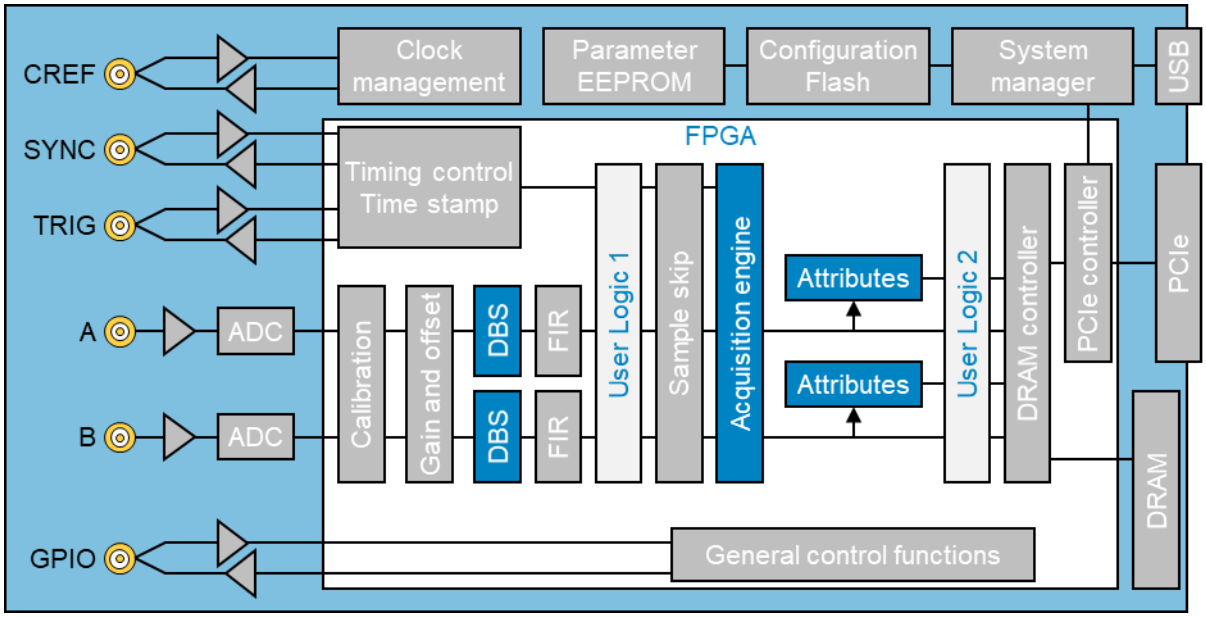

Figure 4 Block diagram for FWPD installed on a dual-channel digitizer.

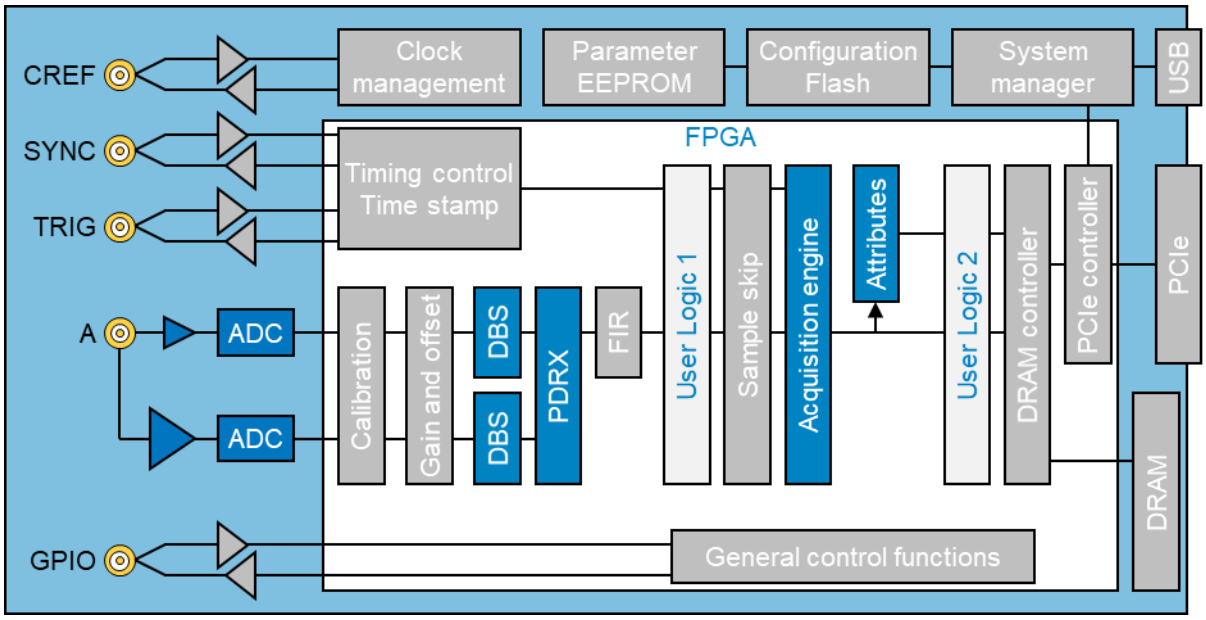

Figure 5 FWPD combined with PDRX, illustrated with channel combination activated.

Figure 6 Typical digitizer in the ADQ3 family.

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